LISTING OF CLAIMS:

1. (Currently Amended) A method for designing buffer and wire placement in an integrated circuit, the method comprising:

representing the surface of a integrated circuit design as a tile graph;

receiving an allocation of buffer locations for selected tiles in the tile graph;

routing nets between a source and one or more associated ~~sources and~~ sinks; and

selectively assigning buffer locations within selected tiles based upon buffer needs of the nets, wherein the nets are routed through selected tiles and assigned buffer locations using a cost minimization algorithm, and wherein a cost array of the cost minimization algorithm for buffer placement is computed using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one associated sink.

2. (Original) The method as recited in claim 1, the step of routing nets between associated sources and sinks comprises:

constructing a Steiner tree for each net to determine congested regions; and

rerouting some of the nets in the congested regions to reduce wire congestion.

3. (Original) The method as recited in claim 2, wherein the rerouting some of the nets comprises minimizing the cost of placing a wire across a tile edge wherein the cost is the number of wires that will be crossing the tile edge divided by the number of wires still available for allocation.

4. (Original) The method as recited in claim 1, further comprising:

rerouting and reallocating some of the nets and buffers to reduce wire and buffer congestion and to reduce the number of nets that have failed to meet their length constraint.

5. (Currently Amended) The method as recited in claim 1, wherein the selectively assigning step ~~of inserting buffers onto nets~~ includes computing a cost, $q(v)$, for using a buffer in a particular tile and the cost, $q(v)$, is given by the equation:

$$q(v)=\begin{cases} \frac{p(v)+c(v)+1}{B(v)-b(v)} & \text{if } \frac{b(v)}{B(v)}<1 \\ \infty & \text{otherwise} \end{cases}$$

wherein $p(v)$ is a sum of probabilities for tile v over all unprocessed nets, wherein $b(v)$ is a current number of used buffer sites, and wherein $B(v)$ is a number of buffer sites in tile v.

6. (Original) The method as recited in claim 5, further comprising:

computing a cost array for buffer placement for a particular net; wherein

each possible arrangement of buffers is represented by an element in the cost array;

each element in the array is the sum of costs, $q(v)$, for one possible arrangement of buffers; and

buffer placement for the particular net corresponds to cost array element having the smallest value.

7. (Original) The method as recited in claim 6, the step of computing the cost array is performed for each net in the integrated circuit.

8. (Currently Amended) The method as recited in claim 1, wherein the ~~plurality of~~ selected tiles [[is]] are less than the total number of tiles in the tile graph.

9. (Currently Amended) A computer program product in a computer readable media for use in a data processing system for designing buffer and wire placement in an integrated circuit, the computer program product comprising:

first instructions for representing the surface of a integrated circuit design as a tile graph;

second instructions for receiving an allocation of buffer locations for selected tiles in the tile graph;

third instructions for routing nets between a source and one or more associated ~~sources and~~ sinks; and

fourth instructions for selectively assigning buffer locations within selected tiles based upon buffer needs of the nets, wherein the nets are routed through selected tiles and assigned buffer locations using a cost minimization algorithm, wherein a cost array of the cost minimization algorithm for buffer placement is computed using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one associated sinks.

10. (Original) The computer program product as recited in claim 9, the third instructions comprise:

fifth instructions for constructing a Steiner tree for each net to determine congested regions; and

sixth instructions for rerouting some of the nets in the congested regions to reduce wire congestion.

11. (Original) The computer program product as recited in claim 10, wherein sixth instructions comprise minimizing the cost of placing a wire across a tile edge wherein the cost is the number of wires that will be crossing the tile edge divided by the number of wires still available.

12. (Original) The computer program product as recited in claim 9, further comprising:

fifth instructions for rerouting and reallocating some of the nets and buffers to reduce wire and buffer congestion and to reduce the number of nets that have failed to meet their length constraint.

13. (Currently Amended) The computer program product as recited in claim 9, wherein the selectively assigning step ~~of inserting buffers onto nets~~ includes computing a cost, $q(v)$, for using a buffer in a particular tile and the cost, $q(v)$, is given by the equation:

$$q(v) = \begin{cases} \frac{p(v) \cdot r_{v(v)+1}}{B(v)-b(v)} & \text{if } \frac{p(v)}{B(v)} < 1 \\ \infty & \text{otherwise} \end{cases}$$

wherein $p(v)$ is a sum of probabilities for tile v over all unprocessed nets, wherein $b(v)$ is a current number of used buffer sites, and wherein $B(v)$ is a number of buffer sites in tile v.

14. (Original) The computer program product as recited in claim 13, further comprising:

fifth instructions for computing a cost array for buffer placement for a particular net; wherein

each possible arrangement of buffers is represented by an element in the cost array;

each element in the array is the sum of costs, $q(v)$, for one possible arrangement of buffers; and

buffer placement for the particular net corresponds to cost array element having the smallest value.

15. (Original) The computer program product as recited in claim 14, wherein the fifth instructions are performed for each net in the integrated circuit design.

16. (Currently Amended) The computer program product as recited in claim 9, wherein the ~~plurality of~~ selected tiles [[is]] are less than the total number of tiles in the tile graph.

17. (Currently Amended) A data processing system for designing buffer and wire placement in an integrated circuit, the data processing system comprising:

a representation unit which represents the surface of a integrated circuit design as a tile graph;

a buffer placement receiving unit which receives an allocation of buffer locations for selected tiles in the tile graph;

an initial routing unit which routes nets between a source and one or more associated ~~sources and~~ sinks; and

a buffer association unit which selectively assigns buffer locations within selected tiles based upon buffer needs of the nets, wherein the nets are routed through selected tiles and assigned buffer locations using a cost minimization algorithm, wherein a cost array of the cost minimization algorithm for buffer placement is computed using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one associated sinks.

18. (Original) The data processing system as recited in claim 17, the third instructions comprise:

a Steiner tree construction unit which constructs a Steiner tree for each net to determine congested regions; and

a rerouting unit which reroutes some of the nets in the congested regions to reduce wire congestion.

19. (Original) The data processing system as recited in claim 18, wherein rerouting unit minimizes the cost of placing a wire across a tile edge wherein the cost is the number of wires that will be crossing the tile edge divided by the number of wires still available.

20. (Original) The data processing system as recited in claim 17, further comprising:

a reallocation unit which reroutes and reallocates some of the nets and buffers to reduce wire and buffer congestion and to reduce the number of nets that have failed to meet their length constraint.

21. (Currently Amended) The method as recited in claim 17, wherein the selectively assigning step ~~of inserting buffers onto nets~~ includes computing a cost, $q(v)$, for using a buffer in a particular tile and the cost, $q(v)$, is given by the equation:

$$q(v) = \begin{cases} \frac{p(v)\,[b(v)+1]}{B(v)-b(v)} & \text{if } b(v) < B(v) \\ \infty & \text{otherwise} \end{cases}$$

wherein $p(v)$ is a sum of probabilities for tile v over all unprocessed nets, wherein $b(v)$ is a current number of used buffer sites, and wherein $B(v)$ is a number of buffer sites in tile v.

22. (Original) The data processing system as recited in claim 21, further comprising:

a computing unit which computes a cost array for buffer placement for a particular net; wherein

each possible arrangement of buffers is represented by an element in the cost array;

each element in the array is the sum of costs, $q(v)$, for one possible arrangement of buffers; and

buffer placement for the particular net corresponds to cost array element having the smallest value.

23. (Currently Amended) The data processing system as recited in claim [[23]] 22, wherein the computing unit computes the cost array for each net in the integrated circuit design.

24. (Currently Amended) The data processing system as recited in claim 17, wherein the ~~plurality of~~ selected tiles [[is]] are less than the total number of tiles in the tile graph.